WBS 6.5 : Tile Calorimeter Technical Overview

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Conceptual Design Review of the High luminosity LHC Detector Upgrades
National Science Foundation
Arlington, Virginia
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USATLAS TileCal L2 Construction Mgr

- Mark Oreglia, Professor of Physics, The University of Chicago
- Has been a member of ATLAS and the Tile Calorimeter team from the beginning (1995)
- US ATLAS Level-2 Tile Calorimeter Upgrade Construction mgr
  - Was co-leader of the CERN Tile upgrade R&D effort 2012-15
  - Was USATLAS L2 manager for TileCal upgrade R&D 2012-15
  - Authored the TileCal section of the summer 2015 upgrade scoping doc
  - Currently assisting the TileCal Project Leader in orchestrating the upgrade
- Leads the R&D effort at UChicago to design and prototype front-end boards and main control boards for the upgraded electronics
- Previous Experiments: Crystal Ball (SLAC), CCFR (FNAL), OPAL (LEP/CERN)

Outline

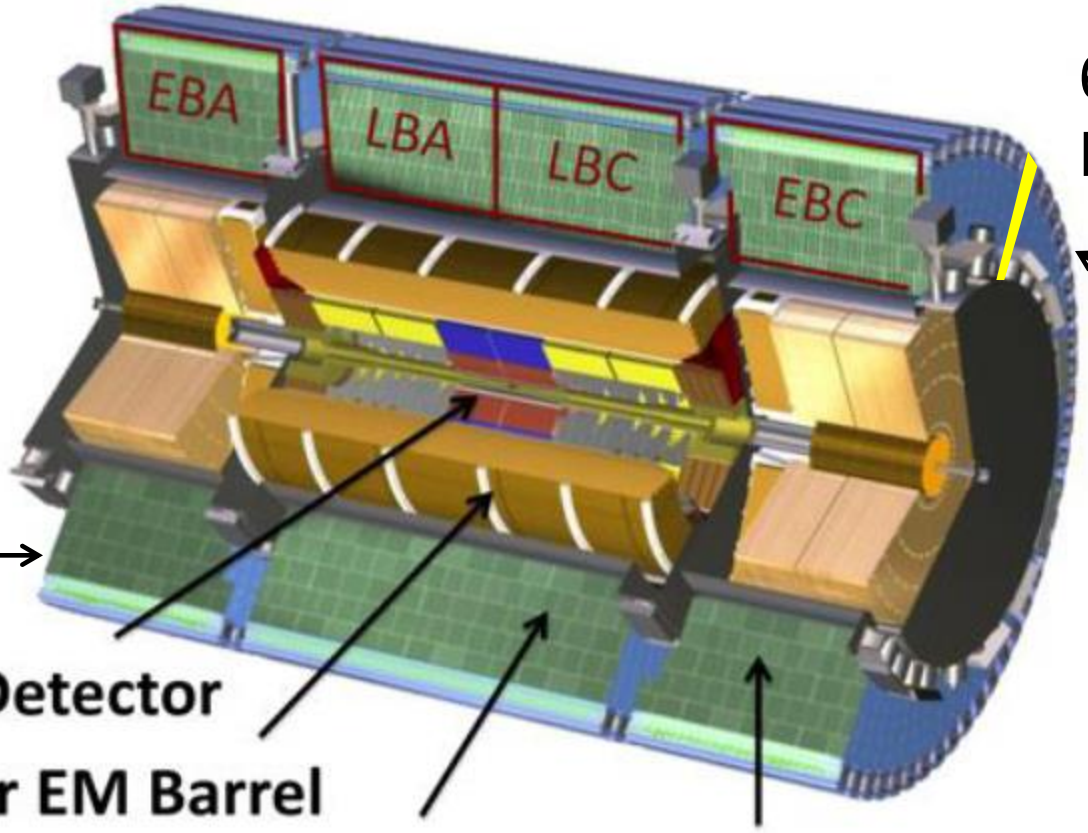
- WBS 6.5: Tile Calorimeter Overview
- Physics and Technical Requirements
- Proposed U.S. HL-LHC Upgrade Scope
- NSF Deliverables
- System Management and Integration
- Milestones, Challenges, Risks
- Ongoing R&D

WBS 6.5: Tile Calorimeter

- This is the outer (hadronic) calorimeter
  - Preceded by LAr EM calorimeter
  - Steel/scintillator calorimeter measures ~35% of jet energy
- Upgrade institutions, WBS-L3, and subsystem managers:
  - University of Chicago, 6.5.1, (UC) Mark Oreglia
    - 6.5.1.1: Main Boards (MB of front-end electronics)
  - University of Texas/Arlington (UTA), 6.5.2, Kaushik De
    - 6.5.2.2: Preprocessor (PPR, back-end DAQ), Giulio Usai
    - 6.5.2.4: Low Voltage “bricks” (LVproduction), Haleh Hadavand
  - Michigan State university, 6.5.3, (MSU) Joey Huston
    - 6.5.3.3: ELMB++ Motherboards (ELMB-MB, LV system)
  - Northern Illinois University (NIU), 6.5.4, Dhiman Chakraborty
    - 6.5.4.2: Low Voltage “boxes” (LVassembly)

The Current Tile Calorimeter

4 “barrels”, 256 modules



64 ϕ Wedges
R: 2.28-3.87m

LV “finger” boxes

D Layer

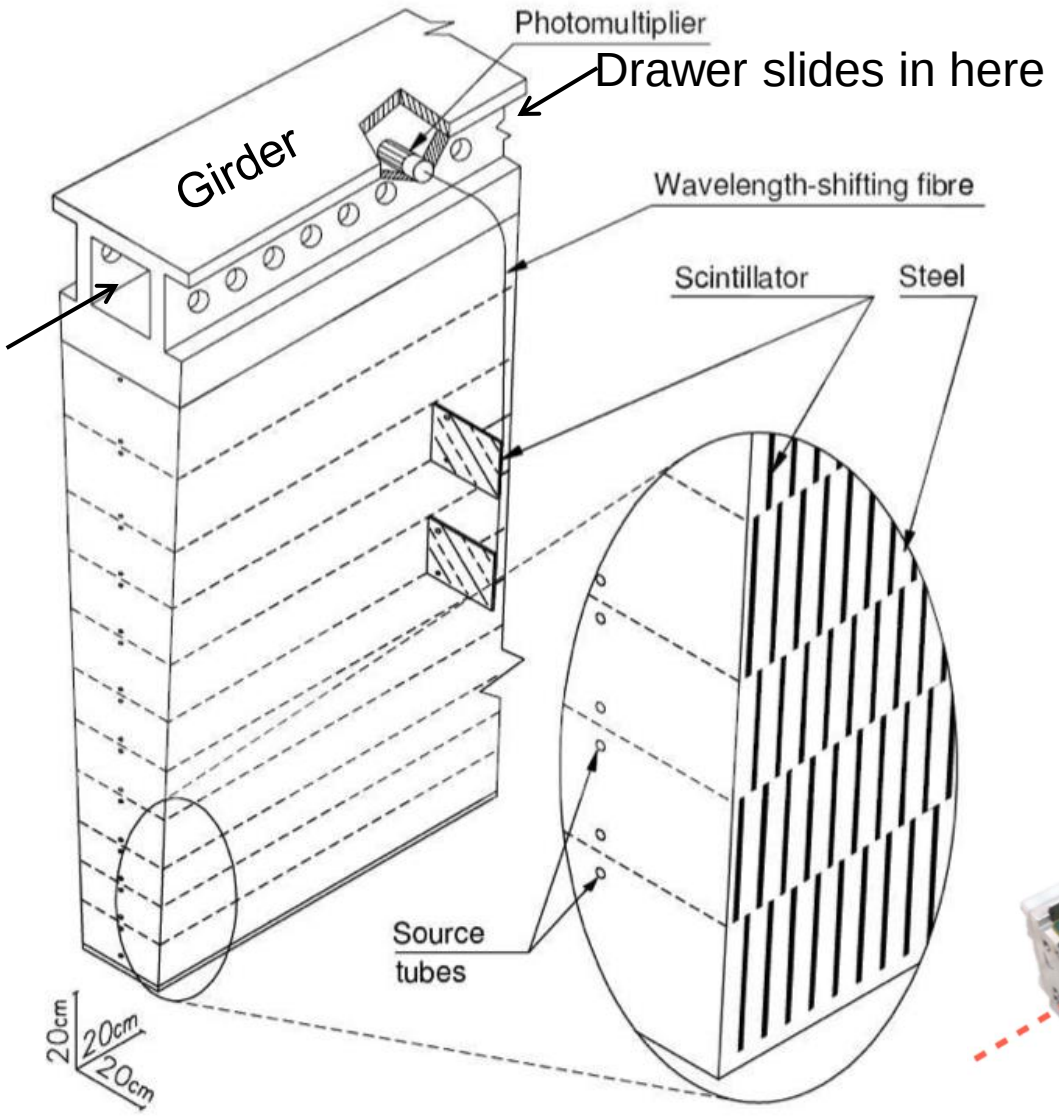
Inner Detector

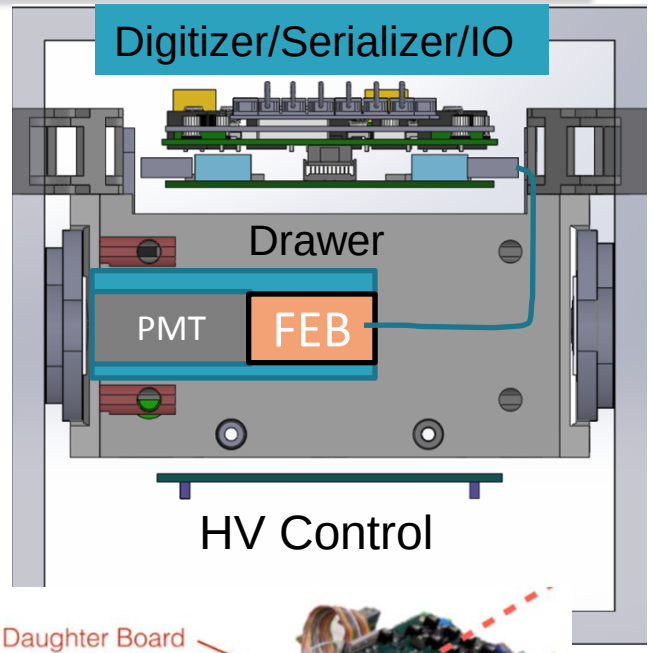
LAr EM Barrel

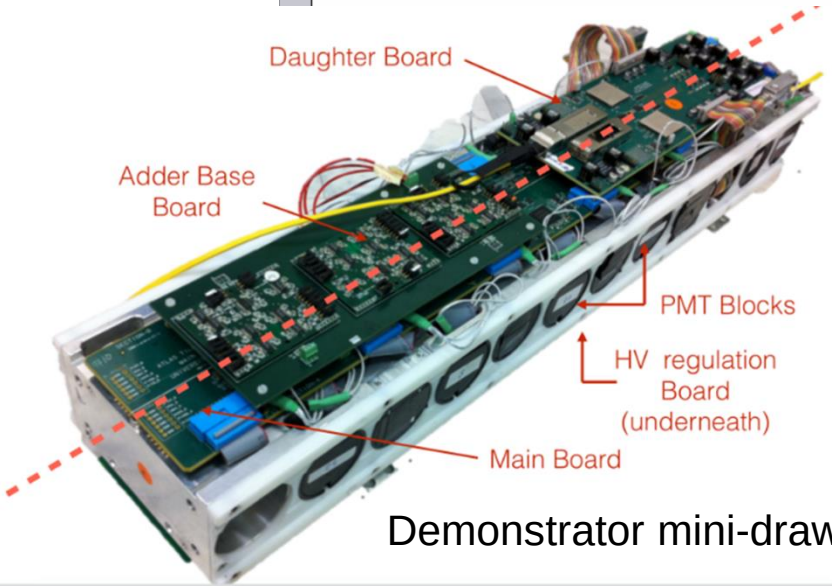
Tile Barrel

Tile Extended Barrel

Tile Wedge Structure







Demonstrator mini-drawer

Physics ⇒ Technology

The Physics mission requires readout of the full granularity of Tile at the 1 MHz L0 trigger rate

SCIENCE GOALS	SCIENCE REQUIREMENTS	NSF SCOPE
$H \rightarrow 4\mu$ (2.2%) VBF $H \rightarrow ZZ^*, WW^*$ (17%,14%) VBS ssWW (5.9%) SUSY $\chi_1^{\pm}\chi_2^0 \rightarrow \ell bb+X$ (850 GeV)	Muon Trigger • single μ p_T threshold ~ 20 GeV • geometric accept: 95% (barrel)	• Muon Electronics • Tile Electronics • sMDT • L0Muon
VBF $H \rightarrow ZZ^*, WW^*$ (17%,14%) VBS ssWW (5.9%) SUSY $\chi_1^{\pm}\chi_2^0 \rightarrow \ell bb+X$ (850 GeV)	Electron Trigger • single e p_T threshold ~ 22 GeV	• LAr+Tile Electronics • L1Global • L1Track/FTK++
HH → 4b (4.4σ KK Graviton)	Jet Triggers • 4-jet E_T threshold ~ 75 GeV • "fat" jet threshold ~ 375 GeV • jet-vertex confirmation at L1	• Lar+Tile Electronics • L1Global • L1Track/FTK++
Compressed SUSY ($\chi_1^{\pm}\chi_2^0$)	Missing E_T Trigger • ME_T threshold ~ 200 GeV • track-based ME_T correction	• Lar+Tile Electronics • L1Global • L1Track/FTK++

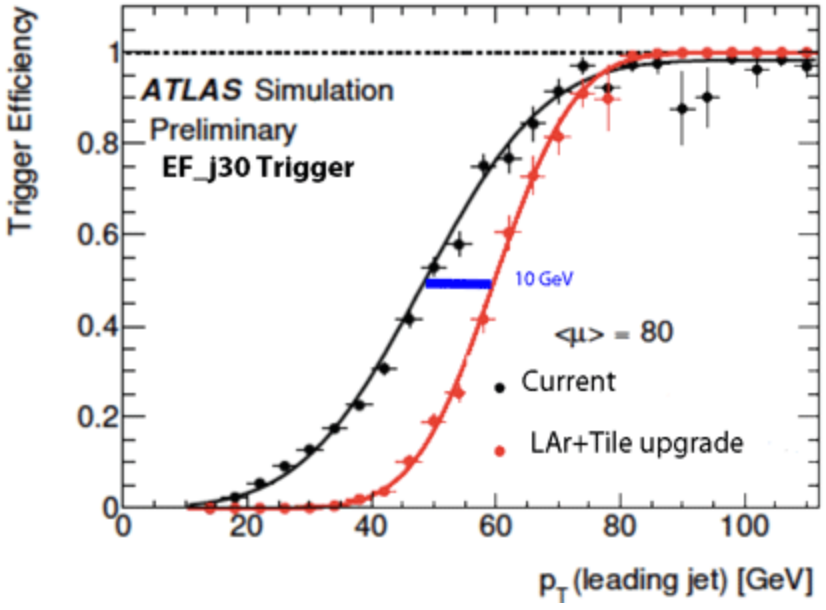
Cost-Effective Trigger System that meets Science Requirements:
- <L0 accept>=1 MHz (6/10μs); <L1 accept>=400 kHz (30/60μs); <to storage>=10 kHz

More Physics and Technical Motivation

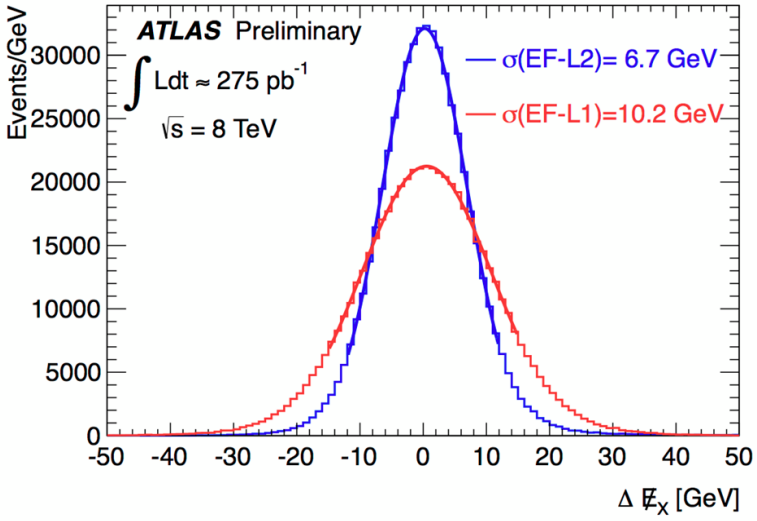
- Physics Motivation:
  - Energy resolution impacts jet rates and physics analysis:
    - ~400MeV noise on current copper trigger lines $\Rightarrow$ optical Tx
    - pileup: get better resolution by storing energies from all cells
      - get longitudinal profile too
  - Missing Energy: dead cells bad for searches
    - increase redundancy and reliability
    - reduce Single Event Upsets
  - Trigger: use information from all cells and configure smart fast triggers in back-end
  - Therefore, send all cell data off-detector: requires new front- and back-end electronics
- Technical Motivation:
  - Radiation: harden electronics, increase redundancy
    - Each drawer ϕ-half completely independent, has separate:
      - 10 volt feed, FPGA and uplink; one half can take over from the other
    - ALARA-driven safer drawer mechanics: 69cm units instead of 140cm
  - Configurable Trigger
    - Send all cell energies to pre-processor
  - NB: the scintillator tiles and PMTs do not require upgrade

2 Examples: Physics Impact

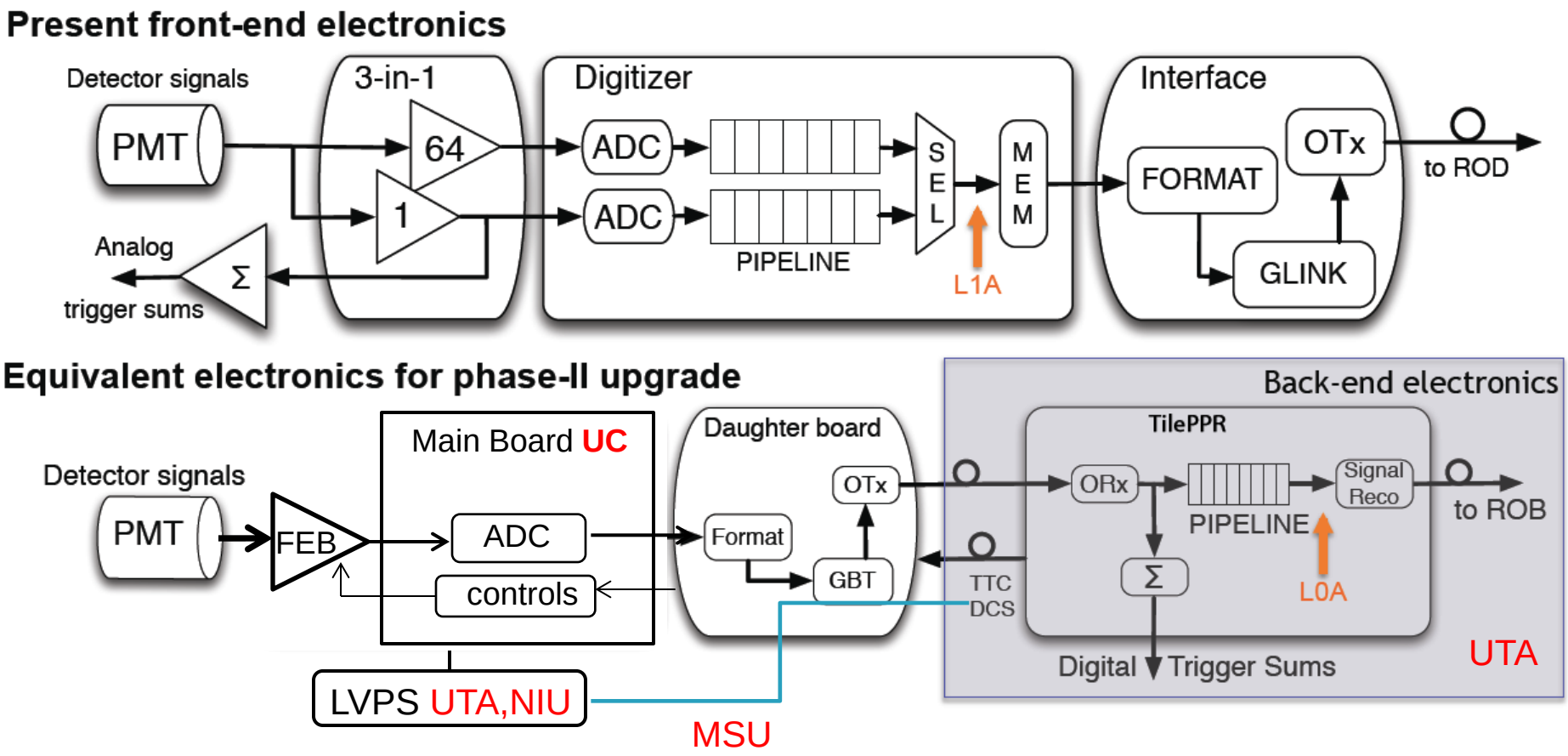
- Jet Trigger Rate
  - Energy resolution improved:
    - lower noise
    - better pileup handling
  - factor 10 improvement in trigger rate



- Missing Energy Resolution
  - Inability to read-out digital data at 40 MHz will hugely impact missing-Et and Ht triggers.
  - Here are distributions when missing-Et is calculated with the analog sums (L1) and digital data (L2):
  - You can see that the digital data gives much smaller noise to missing-Et.
  - The improvement is much higher at \mu=200.



New vs Old Electronics



NB: New electronics already prototyped (“Demonstrator”)

International ATLAS Tile Scoping, Identification of Expertise

- 2012 LOI and 2015 scoping established the full scope of needed Tile upgrade
- Tile Institute Board has agreed on undertaking of upgrade tasks by the traditional Tile institutions:

- good match between interest and expertise
- unofficial money-matrix covers the scope adequately
- Agreements on task sharing were made

Item	Intentions/Interests for production
Mini-drawers	Romanian cluster, IFAE, Clermont consulting
LVPS	UTA, Pisa, Prague AS and CU (ANL consulting), MSU (ELMB)
Active Dividers	To be found, Testbench to be handed by Clermont
FEB+MB	Chicago, Clermont shared In half in items (ANL consulting)
DaughterBoard	Stockholm
HV system	LIP, Prague AS and CU (to specify item) + Clermont help + ANL consulting(if HV opto)
TilePPr, i/f to TDAQ	Valencia, Wits, UTA
New DCS	LIP, MSU (also for ELMB developments)
PMT block	Dubna + to be found
PMTs robustness	Pisa, [Yerevan], UTA (have lifetime bench), Clermont
Optics	counters: Dubna, Wits, Protvino, CERN, MSU; fibers: LIP
MA-PMTs	Dubna, Minsk, CERN, Protvino, ANL(S.Ch), Pisa, MSU, UTA, synergies w/ ALFA
Laser system	Clermont (consulting), Pisa, LIP, CERN
Cs system	Protvino, CERN

US/NSF Deliverables

- 6.5.1.1 (UC): Main Boards of front-end system
  - designed old and new front-end systems (demonstrator)
- 6.5.2.2 (UTA-1): Pre-processor TDAQi (interface boards)
  - has expertise in original "ROD" preprocessor and development of demonstrator back-end electronics
- 6.5.3.3 (MSU): motherboards for LV control
  - experts on Detector Control Systems since the beginning
- 6.5.2.4 (UTA-2): LV Power System (50% of LV "bricks")
- 6.5.4.4 (NIU): LV Assembly (50% of LV "boxes")
  - US redesigned LV system after original system started failing; vast improvement

ATLAS WBS	ATLAS Item (Scoping Doc)	US WBS	Deliverable	NSF Fraction Design	NSF Fraction Production
4	**Tile Calorimeter**	**6.5**	**Tile Calorimeter**		**21%**
4.1	**Drawer Mechanics**				**-**
4.1.1	Mini-drawers				-
4.1.2	Tools/Mechanics				-
4.2	**On-detector Electronics**				**32%**
4.2.1	PMT Dividers				-
4.2.2	FE Boards				-
4.2.3	Main Boards	6.5.1.1	Main Boards	100%	100%
4.2.4	Daughter Boards				-
4.2.5	LVPS System				53%
	ELMB++				-
	ELMB++ Motherboards	6.5.3.3	ELMB++ Motherboards	100%	100%
	LVPS	6.5.x.4	LVPS	100%	50%
4.2.6	HV System				-
4.3	**Off-detector Electronics**				**18%**
4.3.1	TilePPR				-
	TilePPr				-
	Tile TDAQi	6.5.2.2	TDAQi	100%	100%
4.4	**Infrastructure**				**-**
4.4.1	Services				-

US/NSF scope amounts to 21% of Tile Upgrade

WBS Definitions 6.5.x.1,2

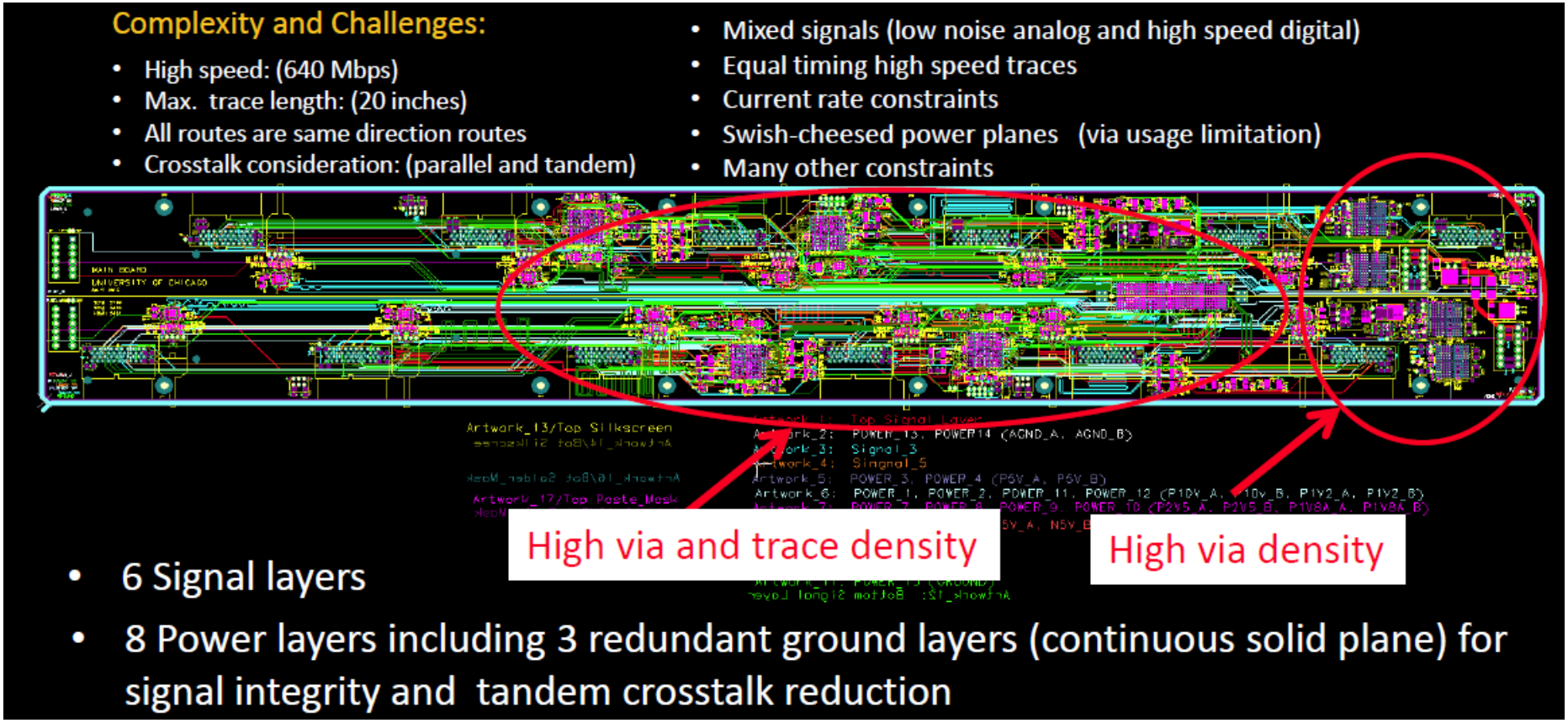
WBS #	WBS Title	WBS Dictionary	Level 2 Manager	Collaborating Institution	Funding Source
6.5	Tile Calorimeter	Replacement of readout and associated electronics for the Tile Calorimeter. US deliverables include: develoment of the Main Board, which houses front-end readout electronics; design and construction of data I/O transition modules for use with the Tile Pre-Processor boards; ELMB++ motherboards used in the collection of monitoring data from the detector and electronics; and production and assembly of the TileCal Low Voltage Power Supply system.	M. Oreglia (Chicago)	-	-
WBS #	WBS Title	WBS Dictionary	Deliverable PI	Collaborating Institution	Funding Source
6.5.1.1	Main Boards	This WBS covers the fabrication of main boards (MB) which manage the data flow, power distribution, monitoring, and calibrations of the Tile Calorimeter front-end electronics. This MB is more radiation tolerant than the current ones, which is a requirement for HL-LHC running. The deliverable for WBS 6.5.1.1 is production of 1,100 boards. Additional tasks are parts procurement and monitoring of outsourced assembly, elevated temperature burn-in of cards with testing and repair, and assembly on the "drawer" mechanical structure for acceptance testing at CERN.	M. Oreglia (Chicago)	Chicago	NSF
6.5.2.2	Preprocessor Interface Boards	This WBS covers the design and fabrication of the Trigger DAQ interface (TDAQi) blades which are the rear transition modules of the Tile calorimeter back-end preprocessor (PPR). These boards configure the processed data from the front-end electronics and route data to the DAQ system via the FELIX module and to the L0/L1 Calo and Muon trigger system through dedicated links. The deliverable for WBS 6.5.2.2 is production of 32 boards. Additional tasks are parts procurement and monitoring of outsourced assembly, burn-in of cards in a dedicated setup with validation testing and repairs when needed.	K. De (UTA)	UTA	NSF

WBS Definitions 6.5.x.3,4

WBS #	WBS Title	WBS Dictionary	Deliverable PI	Collaborating Institution	Funding Source
6.5.3.3	ELMB++Motherboard	This WBS covers the design and fabrication of the motherboard for the new ELMB++ board to be designed for the Tilecal HL-LHC running. The ELMB++ (and its motherboard) is an integral part of DCS control for the Tilecal. The plan is for the new ELMB++ board to allow for greater diagnostic capability for Low Voltage Power Supply failures. The new motherboard, which is mounted in the LV finger box, has to be capable of supporting those new features. The deliverables for WBS 6.5.3.3 are: (1) design of a new motherboard, (2) prototyping of that board, (3) design and production of test equipment for the motherboard, (4) production of 256 ELMB++ motherboards boards over a two-year period, and (5) follow-up of the integration of the ELMB++ motherboards in the Tilecal LVPS system. Items 1 and 2 are not part of project costs, but will be covered by prototyping/R&D funding. Additional tasks are parts procurement and monitoring of outsourced assembly, elevated temperature burn-in of cards with testing and repair.	J. Huston (MSU)	MSU	NSF
6.5.2.4, 6.5.4.4	Low Voltage Power Supply	This WBS covers the production of the Low Voltage Power Supply for the ATLAS Tile Calorimeter HLLHC upgrade. This version of the LVPS consists of +10 volt modules (bricks); 8 of these bricks are mounted in LVBOXes which are mounted at the end of each Tile Calorimeter drawer. 256 of these boxes are needed for the full calorimeter. The primary deliverable for WBS 6.5.2.4 is production of half (1040) of the total number of bricks and half (130) of the LVBOXes ; about 1,140 bricks are produced to account for anticipated yield of 90% over a two-year period. Additional tasks include parts procurement, PCB assembly (outsourced), testing of the bricks at standard and elevated temperature (Burn-in), and repair of faulty bricks. The bricks will be shipped to NIU for inclusion in boxes of eight, tested and shipped to CERN. A transition period from ANL to UTA including	A. Brandt (UTA) H. Hadavand (UTA) D. Charaborty (NIU)	UTA UTA NIU	NSF NSF NSF

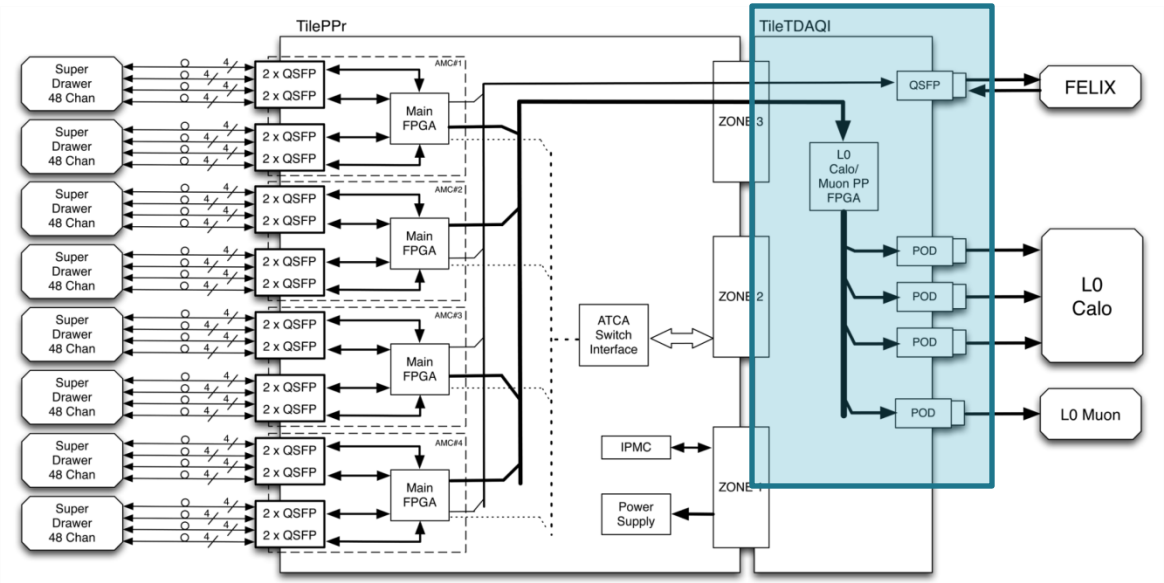
6.5.1.1: Main Board (UC)

- interface between FE amplifier/shaper and fast communications DaughterBoard
- 69 cm length , 16 layer board; 1024 needed
- Supplies LV levels, controls, digitization
- into 3rd prototype version for demonstrator

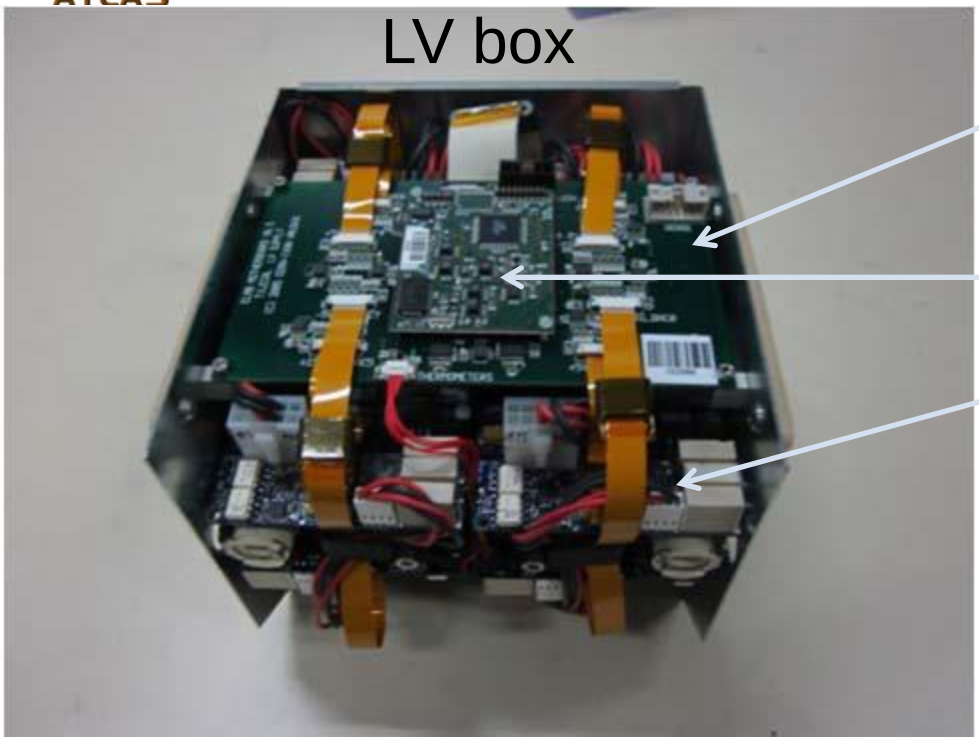


6.5.2.2: Pre-Processor TDAQi (UTA-1)

- PPr + TDAQinterface: receive the ADC raw data, process/calibrate, route data
- TDAQi = smart rear transition module on back-end PreProcessor
  - routes processed cell data to DAQ system
  - send reduced data to trigger processors
- UTA will produce all 32 boards needed
- UTA has long involvement in sROD (PPR) maintenance, debugging
- PPR front-end prototyped for demonstrator; TDAQi designed and costed



6.5.3.3: ELMB++ Motherboard (MSU)



- Motherboard with ELMB handles communication between LVbox and Detector Control System
  - set voltages
  - monitor current, temperature

- MSU proposes to design and make all 256 motherboards needed for LV system
- MSU has had longtime role in Tile control systems
- is starting work with CERN to specify ELMB++ specs

6.5.x.4: LVPS (UTA,NIU)

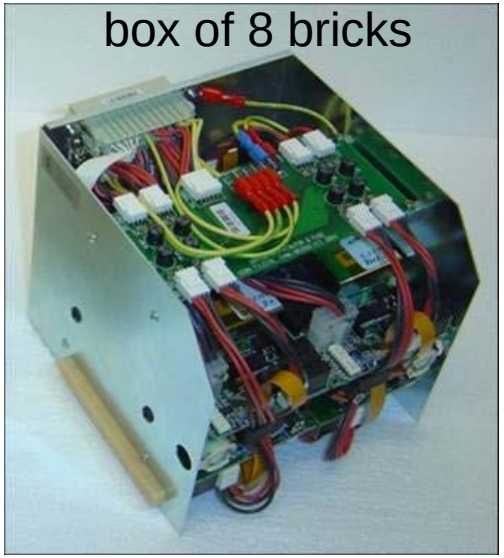
UTA makes 50% of bricks; NIU makes/assembles 50% of boxes

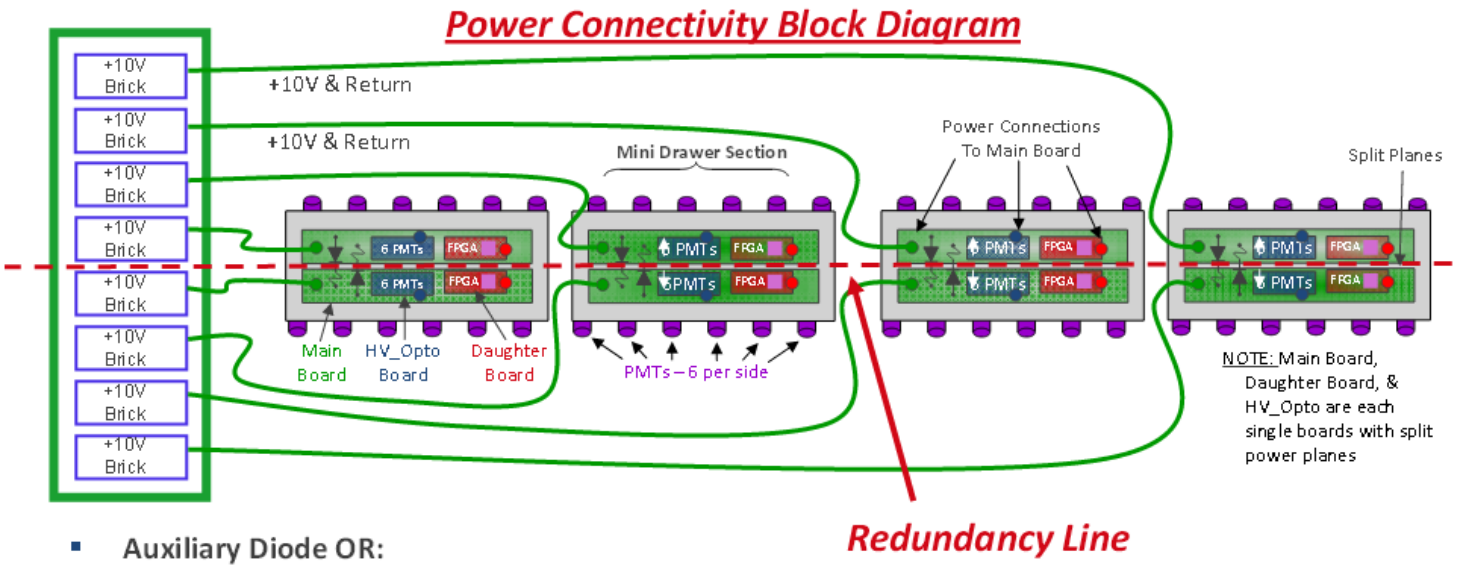
One 10v brick

Each brick supplies 10v to half of a Main Board to feed point of load regulators

- US-designed system
- Board fabricated by vendor
- Burned in and tested at UTA
- NIU:
  - makes boxes
  - assembles with bricks
  - attaches ELMB MB
  - tests

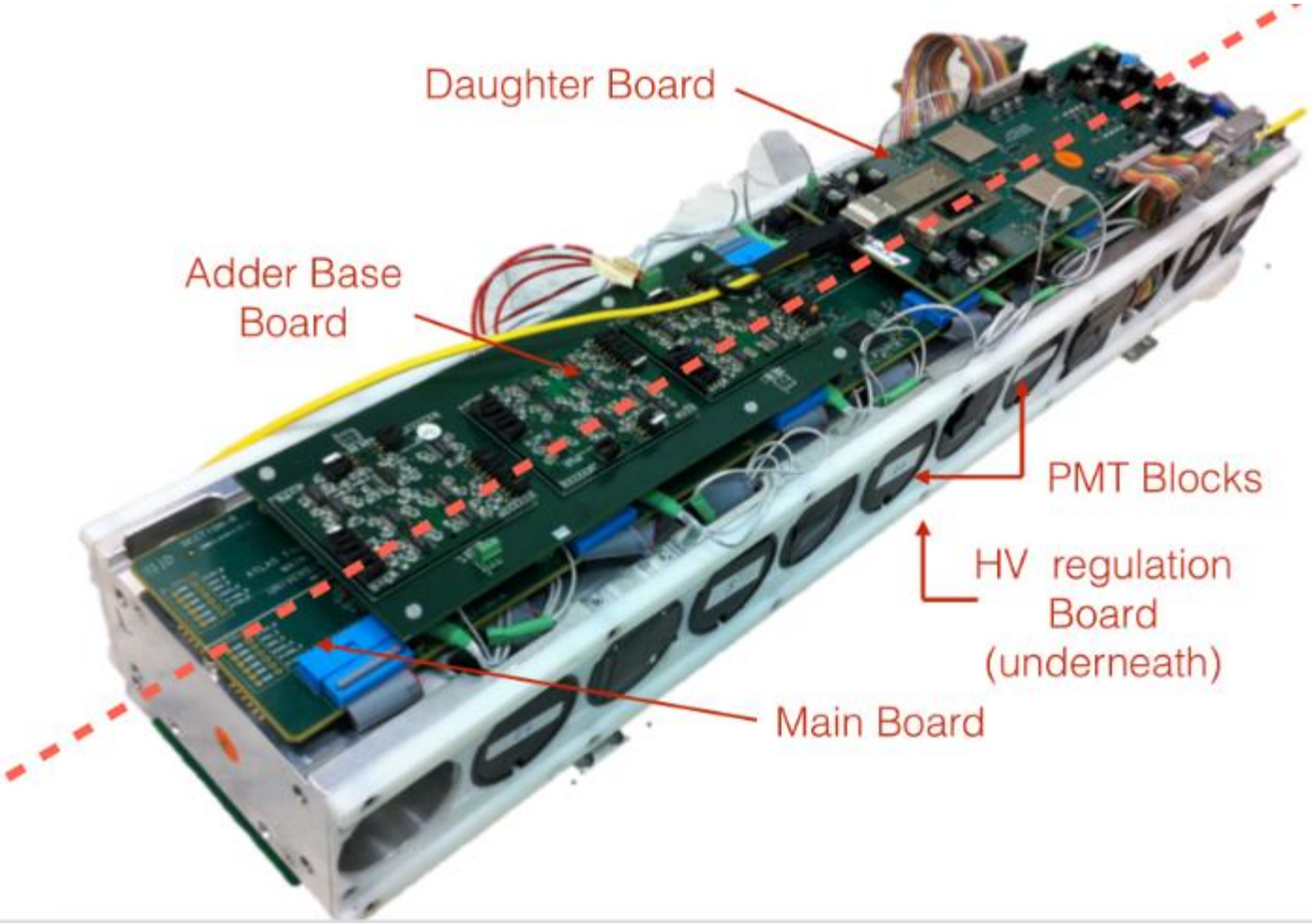
box of 8 bricks





- Auxiliary Diode OR:

R&D: Demonstrator Mini-drawer



Research and Development

The Demonstrator Program

- R&D from USATLAS to build and evaluate demonstrators
  - 3in1, QIE front-end cards and Main Boards produced for demonstrator
  - LV, HV control boards designed and prototyped; LVboxes produced
  - Radiation certification of components and development of rad-hard optical modulator
- Good progress so far:
  - 2015: beam test of 3in1-based demonstrator (successful!)
  - 2016: two more beam tests to evaluate ASIC FEB's
  - 2016: simulations; which FEB handles pileup best?
  - 2017: experience with a demonstrator in ATLAS detector
  - 2017-2020: final integrated design, prototype, testing
    - Includes test beam running to measure Jet Energy Scale and radiation certification

Pending Downselect:

Front-end amplifier/shaper board (FEB)

- Chicago's 3in1 FEB and associated Main Board are the **default**
  - Performing well in tests and radiation certification
  - Most complicated MB (has ADCs); total MB cost ≈ total FEB cost
  - Shapes pulse and has dual gain ranges
- Two ASIC alternatives being evaluated
  - QIE (ANL): boxcar integrator, 5 gain ranges
  - FATALIC (LPC Clermont-Ferrand): shaped pulse, 3 gain ranges
  - Downselect: by end of CY 2017
- Whatever alternative is chosen, UChicago and LPC will share:
  - Chicago makes the Main Boards (simpler for the ASIC alternatives)
  - LPC manufactures the front-end cards
    - This makes sense especially if an ASIC is used (single point of contact)

System Integration

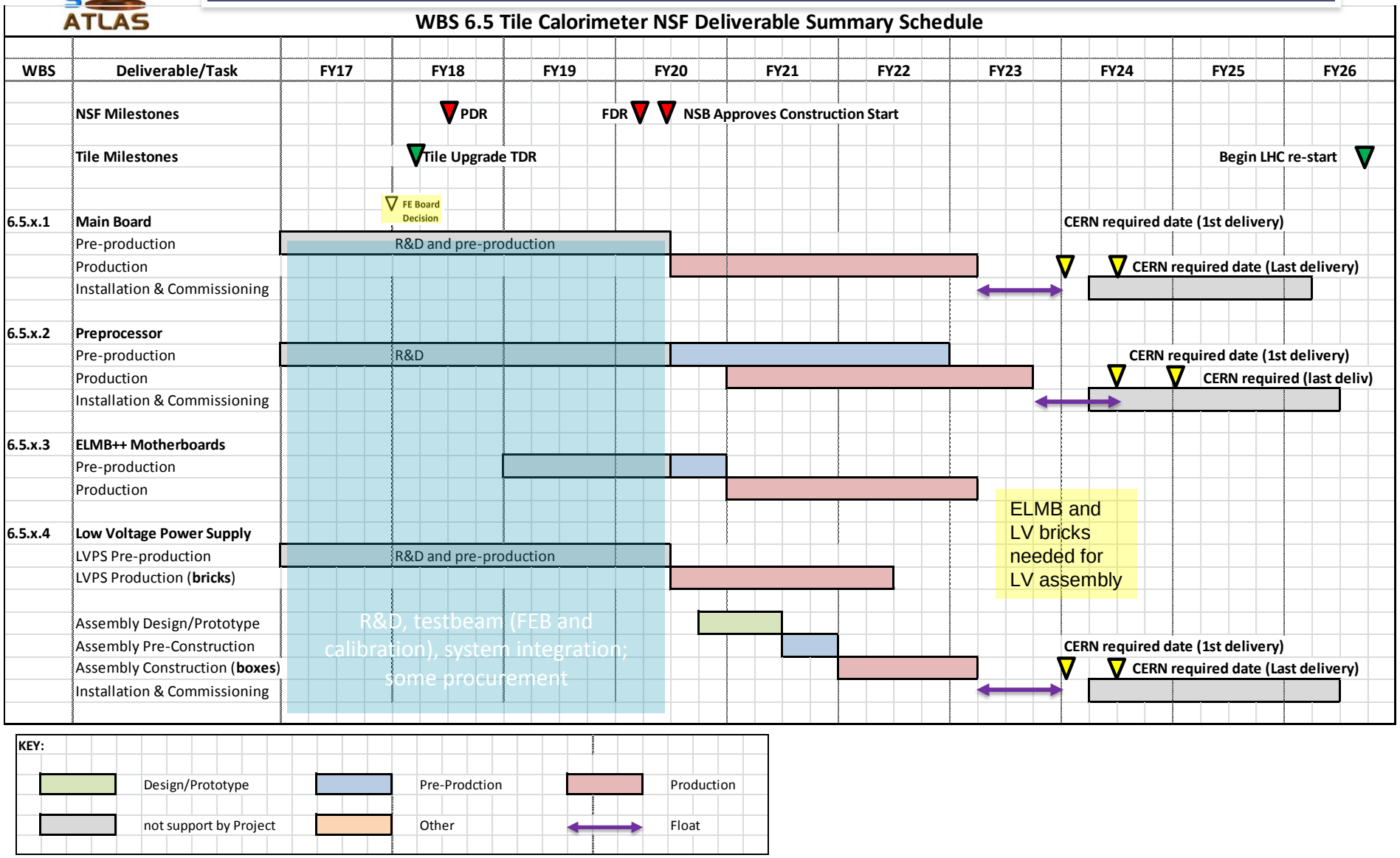
- Gary Drake, EE at UC and ANL, has been asked to act as Integration Engineer for Tile
  - He has long-time knowledge of Tile electronics
  - He designed and produced the new LV system in current detector
  - Since 2012 he has been the Project Manager for the CERN Tile Upgrade R&D (Demonstrator Project)
- Gary's contributions were an important reason for the progress and success we have had in the demonstrator project
- Main Responsibilities:
  - Organize "Expert Weeks" during R&D and pre-production era
  - Organize reviews of final design and check that CERN requirements have been satisfied
    - TDAQ specs; radiation certification
  - Monitor schedule, identify problems and ensure they are addressed
  - Interact with international ATLAS/Tile
  - Oversee delivery to CERN and acceptance testing

Risks

- Risks all low because of working demonstrator prototype
- Cost risk: very low
  - have BOMs from demonstrator; cost goes down for CERN bulk purchases
  - only assuming 20% bulk discount from retail (it's usually higher)
  - FPGAs likely to go down in cost; we are using quotes for FY18
- Schedule risk: low
  - not negligible, because Tile installation is early in the schedule
  - but significant float in proposed schedule (12-19 months)
- Technical risk: very low
  - Tile is in lower radiation area
  - electronics design not too sophisticated; often similar to current design
  - main risk: replacement component does not meet radiation standard

Level 4 Timeline

Driven by CERN Scoping Document and installation schedule



External Dependencies

no showstoppers

- MB: burn-in to be done with front-end cards supplied by Clermont
  - Could use cards from demonstrator for MB production
- PPR: - no external dependency –
- ELMB Motherboard: needs ELMB++ chip supplied by ATLAS
  - Could run motherboard testing using ELMB++ surrogate
- LV system: LV box chassis and cold plate supplied by Prague
  - can restructure procurement to make those parts in US for 50% of boxes

Concluding Remarks

- US Deliverables: Main Boards, PPR TDAQi, ELMB-MB/DCS, LVPS
  - developed by US groups with long-time involvement in Tile
  - essential to achieve 1 MHz trigger rate required to address physics
    - and lead to numerous other improvements in the physics
  - already proven by Tile demonstrator project
    - costs and effort well understood ⇒ low risk and well within contingency

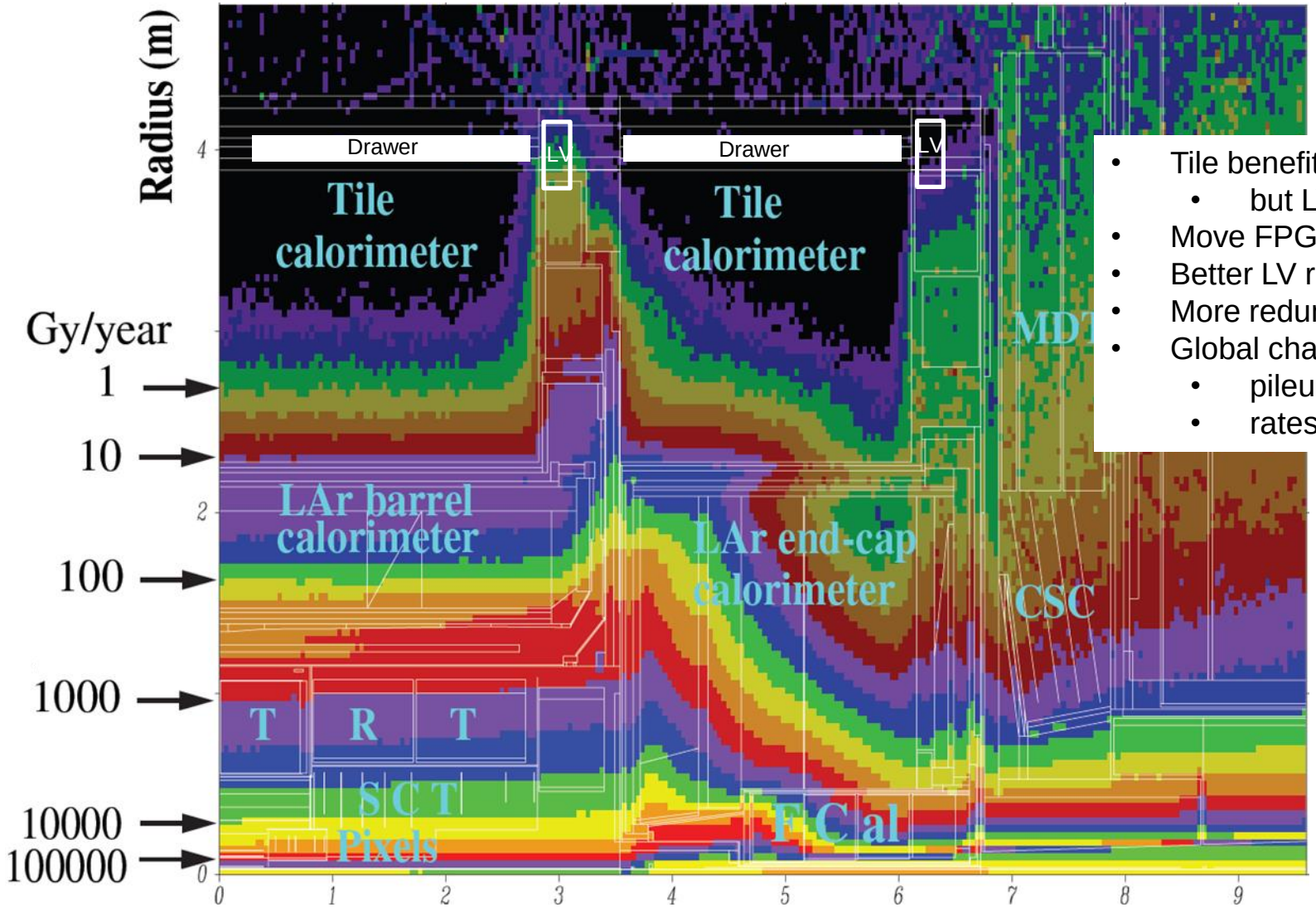
- Total construction cost of $3988K (w/o contingency)
  - 2.8% of total US projects
- Low risks, all mitigable:

Extra Slides

More Motivation to Upgrade

- The present system uses analog sums for real-time triggers and digital data for the higher level triggers. The digital data is available only at 100 kHz.
- The analog trigger sums can not be processed optimally to suppress the out-of-time pileup, partially because the long cables degrade the signal quality and introduce a lot of noise. These sums are needed to trigger on missing momentum, energetic jets, and muon.
- The D-layer is key to reducing the beam-induced backgrounds: https://cds.cern.ch/record/2057719
- Must have the digital readout at 40 MHz to trigger muons in the central (RPC-covered) region, as discussed in the ATLAS scoping document.
- Better energy resolution and pile-up subtraction will have a big impact on missing energy measurement and triggers
- improve calculation of electron/photon leakage into the hadronic calorimeter; used to reject hadron jets faking electrons.
- Better measurement of lepton isolation is key to low-pT thresholds for the lepton triggers.
- digital data to trigger gives you much more flexibility how to process it in the trigger system than the analog sums. This is the basis of the fine-grained Phase-1 trigger processor.

Radiation Map (100 fb^{-1})



- Tile benefits from shielding
  - but LVPS in n-plume
- Move FPGAs in more
- Better LV rad tolerance
- More redundancy
- Global challenges:
  - pileup: μ=140-200
  - rates, latency

Budget Contingency (1)

- 35% for low-risk system, rather conservatively applied:
  - Material Contingency Rule 4 :
    - "25-40% contingency on: items that can be readily estimated from a reasonably detailed but not completed design; items adapted from existing designs but with minor modifications, produced within the previous two years, with documented costs. A recent vendor survey based on a preliminary design belongs here."
    - In fact, parts quotes exist, but purchases to be made in FY20,21.
  - Labor Contingency Rule 3:
    - "25-40% contingency for a task that is conventional, well defined and tends to be repeatable with good confidence but can expect small fluctuations; .for example, testing of production electronics components (most boards take the same unit time, a few take longer); for example, fabrication of multiple similar components but which are not an assembly-line process; for example, design labor for conventional items which offer little to no technical risk."
    - Effort estimate is solid, but assume 2.5% inflation in rates

Budget Contingency (2)

- MB: have BOM's and good estimate of effort from demonstrator (production of 10 Main Boards); supported by actual labor for original motherboard production at UC
- PPR/TDAQi: have good estimate of BOM from PPR+TDAQ demonstrator prototype. Effort well estimated from original ROD production.
- ELMB-MB/DCS: very similar to existing motherboard, and have detailed production estimate from lead engineer.
- LV System: production effort and material virtually identical to 2014 replacement of current LV system. Well documented production plan.

Scope Contingency

- Decision to be made by management, consultation with Int'l ATLAS
- For all subsystems, by late FY21 we will know:
  - actual parts cost
  - failure rate ⇒ repair effort
- If infusion of funds not possible from contingency or Int'l ATLAS:
  - LV box/assembly production 6.5.4.4 would be the easiest deliverable to hand over:
    - comes as last electronics effort; last step in LV system chain
    - most likely US task to find someone else to cover – expertise at Prague
    - recovers $397k (11%)
    - would need to make that decision in CY 2021

Scope Opportunity

- Scope Opportunity … decided by US management
  - LVPS: there are arguments for building 100% in US
    - US undertakes 50% production in current proposal
    - US has proven track record for this
    - Achieve better product consistency
    - Would cost additional $1063K
    - BUT … decision would have to be made by FY21
  - Main Board, if 3in1 front-end board is not chosen:
    - for ASIC FEB the MBs are simpler, cheaper
    - could use the cost recovered to contribute FEB test stands, etc
      - decision by FY21
    - again, a decision to be made by management
    - approximate cost recovery: ~ $400k